TRANSMITTAL OF APPEAL BRIEF (Large Entity)	Docket No. 362-39 RCE

In Re Application Of: **Katsumi Sameshima**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
09/451,979	November 30, 1999	Wai Sing Louie	33769	2714	9727

Invention: **FERROELECTRIC MEMORY AND METHOD FOR MANUFACTURING SAME**

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Gerald T. Bodner

Signature

Dated: October 4, 2004

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant:	Katsumi Sameshima	**Examiner:**	Wai Sing Louie
Serial No.:	09/451,979	**Art Unit:**	2714
Filed:	November 30, 1999	**Docket:**	362-39 RCE
Confirmation No.:	9727	**Customer No.:**	33769
For:	FERROELECTRIC MEMORY AND METHOD FOR MANUFACTURING SAME	**Date:**	October 4, 2004

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Date: October 4, 2004

By: Susan L. Toledano

APPEAL BRIEF

Sir:

Pursuant to the provisions of 35 U.S.C. §134 and 37 C.F.R. 41.37, this paper is submitted as a brief setting forth the authorities and arguments upon which Appellant relies in support of the appeal from the Final Rejection of Claims 1 and 3-5 in the above-identified patent application on December 9, 2003. The Notice of Appeal was duly filed with the appropriate fee on June 3, 2004. A Petition for a two-month extension of time is being filed concurrently herewith.

This brief is in the format specified by the Answer to Comment 61 appearing in the Federal Register, Vol. 69, No. 155, Part II, pages 49978-49979 on August 12, 2004.

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I. REAL PARTY IN INTEREST

The real party in interest in the above-identified patent application is Rohm Co. Ltd., having a place of business at 21, Saiin Mizosaki-cho, Ukyo-ku, Kyoto, Japan.

II. RELATED APPEALS AND INTERFERENCES

No related appeals or interferences are known to the Appellant, Appellant's legal representative, or assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in this pending appeal.

III. STATUS OF THE CLAIMS

Claim 1 stands rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,708,284 (Onishi) in view of U.S. Patent No. 4,737,422 (Knight, et al.).

Claim 2 has been cancelled.

Claim 3 stands rejected under 35 U.S.C. §103(a) as being unpatentable over the Onishi patent modified by the Knight et al. patent as applied to Claim 1, and further in view of U.S. Patent No. 5,861,344 (Roberts, et al.).

Claim 4 has been rejected under 35 U.S.C. §103(a) as being unpatentable over the Onishi patent modified by the Knight et al. patent as applied to Claim 1, and further in view of U.S. Patent No. 6,344,413 (Zurcher, et al.).

Claim 5 has been rejected under 35 U.S.C. §103(a) as being unpatentable over the Onishi patent modified by the Knight et al. patent as applied to Claim 1, and further in view of U.S. Patent No. 5,767,541 (Hanagasaki). Applicant hereby appeals the rejection of Claims 1 and 3-5.

IV. STATUS OF THE AMENDMENTS

Subsequent to the issuance of the Final Rejection of December 9, 2003, Appellant filed, in conjunction with a Notice of Appeal, an amendment in a Reply to Final Office Action mailed on June 3, 2004 to amend Claim 4 to add the word "top" before the word "surface" on line 7 of the claim, the word "top" being added for clarification purposes.

In an Advisory Action mailed on July 7, 2004, the Examiner marked only paragraph 5 that the request for reconsideration has been considered but does NOT place the application in condition for allowance.

In paragraph 2, the Examiner did not indicate whether or not the proposed amendment will be entered. In paragraph 7 of the Advisory Action, the Examiner did not indicate whether, for purposes of Appeal, the proposed amendment will be entered or not entered but only indicated that the claims rejected are Claims 1 and 3-5. In a subsequent telephone interview between Appellant's attorney, Gerald Bodner, and Examiner Louie on October 4, 2004, Examiner Louie stated that the amendment to Claim 4 will not be entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The invention defined by the claims on appeal is directed to a ferroelectric memory, which includes an insulation film 12 having a concave portion or hollow 14 formed at its top surface, and a laminated body obtained by laminating a plurality of layers on the top surface of the insulation film (please see, for example, the specification, as originally filed and as entered by amendment of August 13, 2001 at page 5, line 21 to page 6, line 1, and Figure 1 of the drawings). As will be described in greater detail in this section for each claim, the laminated body includes a plurality of layers on the top surface of the insulation film 12 that are etched in a region corresponding to a region other than the concave portion or hollow 14 (please see the specification, at page 5, line 21, to page 7, line 22, and Figure 1 of the drawings).

With respect to Claim 1, (specification, page 6, line 2, to page 8, line 4, FIGS. 1 – 2) the laminated body includes a lower electrode layer 26 which is made of a gel dry film and which is brought into contact with a bottom surface of the concave portion 14. Claim 1 further calls for the laminated body having a ferroelectric layer 28 formed on the lower electrode layer 26, and an upper electrode layer 30 formed on the ferroelectric layer 28. Claim 1 specifically calls for a portion of the lower electrode layer 26 being only embedded in the concave portion 14 and protruding outwardly from an inner peripheral edge forming the concave portion 14. Claim 1 also specifically defines that portion of the lower electrode layer 26 as having a side which is flush with a side of the ferroelectric layer 28 and with a side of the upper electrode layer 30, so that the sides of the three layers are flush with each other (See Figure 2(E)).

The advantage of having the lower electrode 26 formed in the hollow or concave portion 14 is that the period of time required for the etching process is shortened, which substantially prevents the deterioration of ferroelectric characteristics, as disclosed at page 1, line 25 to page 2, line 9; page 7, lines 3-11; page 7, line 23 to page 8, line 4; and page 9, lines 1-20 of the specification.

Claim 3 (specification, as amended August 13, 2001, page 10, line 6, to page 11, line 2, FIGS. 10-12), which is also in independent form, defines a ferroelectric memory as including an insulation film 12 having a hollow 14 formed at its top surface, and a laminated body obtained by laminating a plurality of layers on the top surface and etching a region of the plurality of layers corresponding to a region other than the hollow 14. Claim 3 specifically defines the laminated body as having a lower electrode layer 26, a ferroelectric layer 28 formed on the lower electrode layer 26, and an upper electrode layer 30 formed on the ferroelectric layer 28. Claim 3 further defines the lower electrode layer as including a first electrode portion 16a formed by a sol-gel technique only at a corner of the hollow 14, and a second portion 16b formed on the first electrode portion 16a. As disclosed on page 10, lines 6-19 of the subject application, with this particular structure, the amount of depression which may result in the center of the top surface of the second electrode portion 16b may be decreased when the lower electrode 16 is baked.

Claim 4 (specification, page 9, line 8, to page 11, line 2, FIG. 8), another independent claim, defines a ferroelectric memory of the present invention as including an insulation film 12 having a concave portion 14 formed at its top surface, and a laminated body obtained by laminating a plurality of layers on the top surface and etching a region of the plurality of layers corresponding to a region other than the concave portion 14. Claim 4 specifically defines the laminated body as including a lower electrode layer 26 which is brought into contact with a bottom surface of the concave portion 14. Also, a thin film 36 of the same material as that of the lower electrode layer 26 is formed on a surface of the lower electrode layer 36 (specification, page 9, lines 17 - 20; Figure 8). The laminated body further includes a ferroelectric layer 28 formed on the thin film 36, and an upper electrode layer 30 formed on the ferroelectric layer 28. Claim 4 also defines a side of the thin film 36, a side of the ferroelectric layer 28 and a side of the upper electrode layer 30 being flush with each other (specification, page 8, lines 15 - 20; Figure 8). The advantage of having a thin film 36 formed on the surface of the lower electrode 26 and using for the thin film 36 the same material as the lower electrode 26 is that it eliminates the surface roughening in the lower electrode 26 which is caused by the planarization process. This is

disclosed at page 9, lines 17 - 20 of the subject application.

Independent Claim 5 calls for a ferroelectric memory having an insulation film 12 with a concave portion 14 at its top surface. The claim also calls for a laminated body obtained by laminating a plurality of layers on the top surface of the insulation film 12 and etching a region of the plurality of layers corresponding to a region other than the concave portion 14. Claim 5 specifically defines the laminated body as including a lower electrode layer 26 which is brought into contact with a bottom surface of the concave portion 14, a ferroelectric layer 28 formed on the lower electrode layer 26, and an upper electrode layer 30 formed on the ferroelectric layer 28 (specification, page 8, lines 8 - 25; Figure 7). Claim 5 further calls for the lower electrode layer 26 and the insulation film 12 at their respective top surfaces being planarized flush with each other, and a side of the ferroelectric layer 28 and a side of the upper electrode layer 30 being flush with each other (specification, page 9, lines 12 - 15; Figure 7). As shown in Figure 7, the film 28 is formed after planarizing the top surfaces of the first conductive film (i.e., the lower electrode layer 26) and the insulation film 12 so that the two will be flush with each other. As a result, the lower electrode layer 26 is entirely buried in the concave portion or hollow 14. As such, the etch time can be further shortened, as it is unnecessary to etch that portion of the first conductive film (i.e., the lower electrode layer 26) which extends out of the concave portion or hollow 14 in the later process. This structure, and the advantages of such, are specifically disclosed at page 9, lines 14-17 of the subject application.

VI. GROUNDS OF REJECTION TO BE REVIEWED UPON APPEAL

Claim 1 is rejected under 35 U.S.C. §103(a) as being unpatentable over Onishi (US Patent No. 5,708,284, issued January 13, 1998) in view of Knight et al., (US Patent No. 4,737,422, issued April 12, 1988).

Claim 3 is rejected under 35 U.S.C. §103(a) as being unpatentable over Onishi modified by Knight et al., as applied to Claim 1, and further in view of Roberts et al. (US Patent No. 5,861,344, issued January 19, 1999).

Claim 4 is rejected under 35 U.S.C. §103(a) as being unpatentable over Onishi modified by Knight et al., as applied to Claim 1, and further in view of Zurcher et al. (US Patent No. 6,344,413 B1, issued February 5, 2002).

Claim 5 is rejected under 35 U.S.C. §103(a) as being unpatentable over Onishi modified by Knight et al., as applied to Claim 1, and further in view of Hanagasaki (US Patent No. 5,767,541, issued June 16, 1998).

The prior art rejections of issue herein apply independently to each claim on appeal, since each claim on appeal is an independent claim. Therefore, none of the claims on appeal stand or fall together with another claim.

The Onishi patent is directed to a non-volatile random access memory which comprises a memory cell including: a MOS transistor having a gate insulation film formed on a semiconductor substrate, a gate electrode, and a pair of impurity diffusion layers; and an MFS transistor having at least a bottom gate electrode, a ferroelectric film, a top electrode, and a pair of impurity diffusion layers, one of the impurity diffusion layers of the MFS transistor being shared with the MOS transistor and connected to a portion of the bottom gate electrode; wherein the MOS transistor is connected to a bit line and a word line, and the MFS transistor is connected to a drive line and a common source line. (Abstract).

The Knight et al. patent is directed to polymer electrolytes incorporated in an electrolytic cell as shown in FIG. 1. A film 1 of the polymer electrolyte is sandwiched between an anode 3 preferably of lithium metal or a lithium alloy, e.g., an alloy with silicon or aluminium, and a cathode 5 comprising e.g., TiS_2 preferably with an added proportion of the electrolyte. The anode 3 and cathode 5 are conventional as is the encapsulation of the cell and/or its assembly within a battery (not shown in FIG. 1). The cell may for example be made up using the techniques described in U.S. Pat. No. 4,303,748. (Column 8, lines 44-56).

The Roberts et al. patent is directed to a method for providing improved step coverage of contacts with conductive materials, and particularly metals. A conductive layer is deposited over an insulating layer, either before or after contact opening formation. After both conductive layer deposition and contact formation, a facet etch is performed to slope the conductive layer overlying the contact lip while depositing material from the conductive layer into the lower corner of the contact, where coverage has traditionally been poor. A second conductive layer may then be deposited into the contact to supplement coverage provided by the first conductive layer and the facet etch. (Abstract).

The Zurcher et al. patent is directed to a method for forming a semiconductor device having an capacitor, where the capacitor is in-laid in a cavity formed in the semiconductor substrate and part of a high density memory. One embodiment first forms a bottom electrode in the cavity and then fills the cavity with a sacrificial layer to allow chemical mechanical polishing (CMP) of at least one of the capacitor electrodes. After removing portions of the bottom electrode and portions of the sacrificial layer, a dielectric layer is formed. A top electrode is then formed over the dielectric layer. The dielectric layer so formed isolates the bottom electrode from the top electrode preventing shorting and leakage currents. In one embodiment, a single top electrode layer is formed for multiple bottom electrodes. (Abstract).

The Hanagasaki patent is directed to a method of manufacturing a semiconductor storage device having a plurality of memory cells each having one transistor and one

ferroelectric capacitor includes the steps of: forming a transistor; forming a plate line; sequentially laminating three layers including a first conductive film, a ferroelectric layer, and a second conductive layer stacked in this order; and sequentially etching the three layers by using a single etching mask. (Abstract)

Accordingly, the first issue presented for review is whether Claim 1 is unpatentable under 35 U.S.C. §103(a) over the Onishi patent in view of the Knight, et al. patent.

The second issue presented for review is whether Claim 3 is unpatentable under 35 U.S.C. §103(a) over the Onishi patent, modified by the Knight, et al. patent as applied to Claim 1, and further in view of the Roberts, et al. patent.

A third issue presented for review is whether Claim 4 is unpatentable under 35 U.S.C. §103(a) over the Onishi patent, modified by the Knight, et al. patent as applied to Claim 1, and further in view of the Zurcher, et al. patent.

A fourth issue presented for review is whether Claim 5 is unpatentable under 35 U.S.C. §103(a) as being unpatentable over the Onishi patent modified by the Knight, et al. patent as applied to Claim 1, and further in view of the Hanagasaki patent.

VII. ARGUMENTS

Claim 1

(A) Claim 1 is patentable under 35 U.S.C. §103(a) and not obvious in view of the Onishi patent and the Knight, et al. patent.

Claim 1 has been rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,708,284 (Onishi) in view of U.S. Patent No. 4,737,422 (Knight et al.). The Examiner contends that the Onishi patent discloses an insulation film 7 having a concave portion at a top surface, a laminated body obtained by laminating a plurality of layers on the top surface and etching a region of the plurality of layers corresponding to a region other than the concave portion, where the laminated body includes a lower electrode 8 which is brought into contact with a bottom surface of the concave portion, a ferroelectric layer 9 formed on the lower electrode 8 and an upper electrode layer 10 formed on the ferroelectric layer 9, where a portion of the lower electrode layer 8 protrudes outward from an inner peripheral edge forming the concave portion, and a side of a portion of the lower electrode layer 8, a side of the ferroelectric layer 9, and a side of the upper electrode layer 10 are flush with each other (the Examiner refers to Figure 6 of the Onishi patent for showing this structure), and a film 8a formed in a bottom of the hollow and separating between the insulating film 7 and the lower electrode layer 8b (the Examiner again refers to Figure 6 of the Onishi patent for showing this structure).

Onishi relates to a method for fabricating a non-volatile memory cell, which includes multiple layers of insulation film formed on a semiconductor substrate, impurity diffusion wells, a bottom gate electrode, a pair of bottom electrode layers, a ferroelectric layer, and a top electrode. As shown in Figure 4, a gate insulation film 2 is formed on the entire surface of a P-type silicon substrate 1, and a first contact hole 4 is formed in the desired region of the gate insulation film 2 by using a resist mask 3.

Next, as shown in Figure 5, an N+-silicon layer is formed over the entire surface of

the semiconductor substrate 1 and patterned into the desired configuration to form the gate electrode 5a and the bottom gate electrode 5b. Phosphorus is diffused from the bottom gate electrode 5b, which is formed within the contact hole 4, into the semiconductor substrate 1 to form an ohmic contact. By using the gate electrode 5a and the bottom gate electrode 5b as a mask, impurity ions are implanted into the semiconductor substrate 1, which is annealed to form impurity diffusion layers 6a, 6b, 6c.

A second interlayer film 7 of non-doped silicate glass is formed over the entire surface of the semiconductor substrate 1, including the gate electrode 5a and the bottom gate electrode 5b. A second contact hole is formed in the second interlayer film 7 on the bottom gate electrode 5b, and a TiN/Ti film 8a and a Pt film 8b, which together comprise the bottom electrode, are deposited over the entire surface of the interlayer film 7. A PZT film 9 serves as a ferroelectric film and is formed on the Pt film 8b.

The lamination of the PZT film 9, Pt film 8b, and TiN/Ti film 8a is etched into the desired configuration. A third interlayer film 7 is formed over the lamination and a third contact hole is formed in the third interlayer film 7 on the PZT film 9. A Pt film is formed on the interlayer film 7 and patterned into the desired configuration as a top electrode 10.

A fourth interlayer film 7 is formed on the top electrode 10 and a fourth contact hole is formed in a fourth interlayer film 7 on the impurity diffusion layer 6b. A bit line 11 made of an aluminum-based material is deposited on the interlayer film 7 including the fourth contact hole to complete the memory cell shown in Figure 1.

The Examiner acknowledges that the Onishi patent does not disclose that the lower electrode layer is made of a gel dry film, which limitation was added in the amendment filed on August 21, 2003. However, the Examiner contends that the Knight, et al. patent discloses forming the lower electrode by vacuum drying a gel solution, and refers to Column 14, lines 57-68 in the Knight, et al. patent for disclosing this feature. The

Examiner further contends that the Knight et al. patent teaches that the gel method could control the physical form and the degree of polymerization of the electrode, at Column 15, lines 13-15, and, therefore, it would have been obvious to modify the Onishi device with the teaching of Knight, et al. to use the gel method to form the lower electrode in order to control the physical form and the degree of polymerization.

U.S. Patent No. 4,737,422 (Knight, et al.), which was the new patent cited by Examiner Louie, was incorrectly cited as showing the formation of the lower electrode by a sol gel technique or for showing that the lower electrode is made of a gel dry film. The Knight et al. reference actually shows the dielectric or ferroelectric layer being formed by a gel method.

With respect to Claim 1, the claim calls for the lower electrode being made of a gel dry film. The Examiner agreed in the Office Action dated December 9, 2003 that the Onishi patent does not disclose this, but he cited the Knight, et al. patent for showing the lower electrode formed by vacuum drying a gel solution.

The Knight et al. patent discloses, at Column 14, lines 57-68, that the dielectric, not the lower electrode, is formed by a gel method. The advantage of using a sol gel technique to form the lower electrode as a gel dry film in the hole 14 is that the precursor which forms the gel dry film is splashed away by centrifugal force, but the precursor in the hole is not splashed away and it remains in the hole. Thus, neither the Onishi patent nor the Knight, et al. patent teaches using a sol gel method to form an electrode as a gel dry film within the hole.

Claim 1 further has the limitation: --wherein a portion of said lower electrode layer is only embedded in said concave portion, and protrudes outward from an inner peripheral edge forming said concave portion, and a side of said portion of said lower electrode layer, a side of said ferroelectric layer and a side of said upper electrode layer are flush with each other.--. Thus, Claim 1 defines the ferroelectric memory as having a lower electrode layer wherein the lower electrode layer is embedded in the concave portion and also protrudes

outwardly from the inner peripheral edge of the insulation film which forms the concave portion.

This structure is an important feature of the claimed invention. After the hollow 14 is formed on the insulation film 12, the first conductive film 26 (i.e., the lower electrode layer), made of the gel dry film is formed by the sol-gel technique on the surface of the first insulation film including on the inside of the hollow 14. That is, the precursor solution is applied onto the surface of the first insulation film 12 by the sol-gel technique, and then dried into the gel dry film. Using the sol-gel technique, the precursor solution dripped on the surface of the first insulation film 12 is splashed away due to the centrifugal force. However, the precursor solution existing inside the hollow 14 will not be readily splashed away. This provides the first conductive film 26 (i.e., the lower electrode layer) with the film thickness that is greater inside the hollow 14 than the other portions outside the hollow, as shown in FIG. 2(B), and disclosed in the specification, at page 6, lines 2-18. The etch process requires the total film thickness of the second conductive film 30 (i.e., the upper electrode layer) and the film 28 (i.e., the ferroelectric layer) to be etched. Advantageously, it is sufficient for the first conductive film 26 to be etched only over portions thereof which extend out of the hollow 14. Therefore, as the etch time is reduced as compared to conventional techniques which require the entire thickness of the lower electrode 16 to be etched, as disclosed at page 7, lines 5-11 of the specification, the time for which the film 28 which forms the ferroelectric layer 18 is exposed to the dry-etching plasma atmosphere is reduced. Therefore, any deterioration to the characteristics of the ferroelectric layer 18 by the effects of the plasma is reduced, as disclosed at page 8, lines 1-4 of the specification.

In contrast, as shown in FIG. 6 of the Onishi patent, the TiN/Ti film 8a and Pt film 8b are deposited over the entire surface of the interlayer film 7 by a sputtering process or CVD process (as described at column 8, lines 15-18 of the Onishi patent). The film thickness of TiN/Ti film 8a and Pt film 8b inside the contact hole is nearly equal to the film thickness at the other portions outside the hole, as shown in FIG. 6 of the Onishi patent. Due to this, the etch time is not reduced, unlike with the structure of the invention

defined by Claim 1. Thus, the ferroelectric in the Onishi structure will be deteriorated in its characteristics, as it is affected by the plasma.

The Knight et al. patent also does not disclose the limitation in Claim 1 of the lower electrode layer having a portion embedded in the concave portion or hollow and protruding outwardly from an inner peripheral edge forming the concave portion or hollow. The Knight et al. patent was only cited (incorrectly) for showing a lower electrode formed by vacuum drying a gel solution. As stated previously, this is not the case, and in fact, the Knight et al. patent discloses polymeric electrolytes for use in electrolytic cells in batteries, which is not even analogous to the art in which the claimed invention resides. The Knight et al. patent shows no structure comparable to an electrode embedded in and extending out of a hole, nor does it address the problems solved by the claimed invention of deterioration to a ferroelectric due to prolonged exposure to the plasma during etching.

A third limitation found in Claim 1 is that the concave portion or hollow 14 is formed in the top surface of the insulation film 12, and the lower electrode layer is brought into contact with a bottom surface of the concave portion or hollow 14. Thus, the concave portion or hollow 14 is formed on the top surface of the insulation film 12, and the laminated body is formed on the concave portion such that the lower electrode layer 16 included in the laminated body contacts with the bottom surface of the concave portion.

In contrast, in the Onishi patent, the contact hole extends entirely down to the bottom gate electrode 5b, and the layer 8b contacts with the layer 8a. More specifically, the contact holes formed through the insulation layers 2, 7 in Figures 1 and 7 of *Onishi* collectively extend entirely down to the substrate. However, in the claimed invention, the concave portion or hollow extends only a portion of the way through the insulation film and does not extend to the substrate. In addition, that portion of *Onishi* relied on by the Examiner (column 8, lines 14-15) indicates that a contact hole is formed in the interlayer film 7 on the bottom gate electrode 5b. Thus, a plurality of layers is not laminated on the top surface of the insulation film in *Onishi*, in contrast to that defined by Claim 1, but rather on the top surface of the bottom gate electrode 5b.

Claim 1 recites that the insulation film includes a concave portion on a top surface of the insulation film, which further clarifies the distinctions between the claimed invention and the contact hole or through-hole described in *Onishi*, which extends completely through the insulation films 2, 7. Therefore, *Onishi* does not describe "an insulation film having a concave portion at a top surface", but rather insulation films with contact holes, as described on column 8, lines 14-15, 24-26, and 30-32, which extend entirely through the insulation films 2, 7 down to the substrate 1.

Thus, in the claimed invention, the laminated body is formed on the concave portion such that the "lower electrode layer is brought into contact with a bottom surface of the concave portion", as defined by Claim 1. In contrast, the contact holes in *Onishi* do not possess a bottom surface since they are holes, not concave portions.

The Knight et al. patent shows no contact holes or hollows whatsoever, and, therefore, like the Onishi patent, does not teach or suggest this particular limitation found in Claim 1.

A fourth limitation found in Claim 1 that is not met by either the Onishi patent or the Knight et al. patent is that a side of the portion of the lower electrode layer, a side of the ferroelectric layer, and a side of the upper electrode layer, are flush with each other. This is clearly shown in the drawings in FIG. 1, FIG. 2(E), FIG. 10 and FIG. 12. However, in *Onishi*, the sides of the upper electrode layer 10, as shown in Figure 7, are not flush with sides of the ferroelectric layer 9, layer 8a, or layer 8b. The Knight et al. patent shows no comparable structure.

Accordingly, it is respectfully urged that Claim 1 patentably distinguishes over the Onishi patent and the Knight et al. patent, alone or in combination, and is therefore allowable. In that the Examiner has failed to establish that Claim 1 is unpatentable over

the prior art, the rejection under 35 U.S.C. 103(a) of Claim 1 as being unpatentable over Onishi in view of Knight et al. is improper, and should be withdrawn.

Claim 3

(B) Claim 3 is patentable under 35 U.S.C. §103(a) over Onishi modified by Knight et al., as applied to Claim 1, and further in view of Roberts et al. (US 5,861,344, issued January 19, 1999).

The Examiner asserts that in addition to the limitations disclosed in Claim 1, Onishi also discloses the lower electrode layer includes a first electrode portion 8a and a second portion 8b formed on the first electrode portion 8a, but Onishi does not disclose the first electrode portion 8a formed only at a corner of the hollow. The Examiner asserts that however, Roberts et al., in column 7, lines 19-30 and FIGS. 3 and 4, disclose forming an improved electrical contact by depositing the corner fill 32. The Examiner further asserts that Roberts et al, in column 2, lines 41-44, teach that the first electrode portion acts as seeding material and selective deposit at the corner and, in column 7, lines 19-23, improves metal contact in the hollow. The Examiner concludes that, therefore, it would have been obvious to one of ordinary skill in the art to modify the teachings of Onishi with the teaching of Roberts et al. to provide the corner fill in the hollow in order to establish the seeding material and improve the metal contact in the hollow.

One of the features of the claim is that the corner electrodes are formed by a sol gel technique, and the advantage of doing this is high accuracy in getting only the corner electrodes formed. The Appellant maintains that the Roberts et al. patent uses a sputter deposition, and Figure 3 in the Roberts et al. patent and the disclosure at Column 6, lines 40-45 show this. In the Roberts et al. device, the conductive corner fill 32 is more difficult to form using this sputter technique, as it uses the upper corner 26 of the first conductive layer 14 as the sputter deposition target. Accordingly, the corner electrodes of the claimed invention are not formed in the same manner as that disclosed in the Roberts et al. patent.

The Appellant maintains that the Knight et al. patent does not teach forming the lower electrode by a sol gel process, and that the Knight et al. patent only describes forming the dielectric or ferroelectric layer by a gel method. The Onishi patent does not show this feature either. Thus, it is respectfully urged that Claim 3 is not taught or suggested by the Onishi patent, the Knight et al. patent and the Roberts et al. patent, alone or in combination, and is therefore allowable.

In that the Examiner has failed to establish that Claim 3 is unpatentable over the prior art, the rejection of Claim 3 under 35 U.S.C. 103(a) as being unpatentable over Onishi in view of Knight et al. and further in view of Roberts et al. is improper, and should be withdrawn.

Claim 4

(C) Claim 4 is patentable under 35 U.S.C. §103(a) over Onishi modified by Knight et al., as applied to Claim 1, and further in view of Zurcher et al. (US 6,344,413 B1, issued February 5, 2002).

Claim 4 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over the Onishi patent modified by the Knight, et al. patent as applied to Claim 1, and further in view of U.S. Patent No. 6,344,413 (Zurcher, et al.). The Examiner acknowledges that the Onishi patent does not disclose that the lower electrode is formed on a surface of a thin film of the same material as that of the lower electrode. However, the Examiner contends that the Zurcher, et al. patent discloses a thin film of titanium which may be deposited on top of the first conductive layer 208, and refers to Column 6, lines 28-43 of the Zurcher, et al. patent for disclosing this structure. The Examiner further contends that the Zurcher, et al. patent discloses that the thin film serves as an adhesion layer, at Column 6, lines 28-43. The Examiner concludes, therefore, that it would have been obvious for one with ordinary skill in the art to modify the Onishi structure in accordance with the teaching of the Zurcher, et al. patent to provide a thin film in the lower electrode in order to approve the adhesion to the lower electrode, and further contends that the first conductive layer 208 is

made of titanium, which is the same material as the thin film.

One of the features in Claim 4 is that the thin film is formed on a surface of the lower electrode 26, and that the thin film is the same material as the lower electrode. The purpose is to eliminate surface roughening on the surface of the planarized lower electrode 26 during the planarization process.

The Onishi patent does not disclose a thin film formed over the lower electrode, each being of the same material, as acknowledged by the Examiner. The Knight et al. patent also does not disclose this structure. More specifically, the Knight et al. patent discloses, in column 8, lines 44-56, the following:

> Polymer electrolytes embodying the first aspect of the invention may be incorporated in an electrolytic cell as shown in FIG. 1. A film 1 of the polymer electrolyte is sandwiched between an anode 3 perferably of lithium metal or a lithium alloy, eg an alloy with silicon or aluminium, and a cathode 5 comprising eg TiS_2 preferably with an added porportion of the electrolyte. The anode 3 and cathode 5 are conventional as is the encapsulation of the cell and/or its assembly within a battery (not shown in FIG. 1). The cell may for example be made up using the techniques described in U.S. Pat. No. 4,303,748.

Therefore, from the above passage, it is clear that the Knight et al. patent does not disclose a thin film formed over the lower electrode, each being of the same material.

The Appellant maintains that the Zurcher et al. patent does not show this feature either. Instead, the Zurcher et al. patent discloses a device in which the adhesion layer, which is not shown, is described as being between the barrier layer 208 and under the first electrode 210. Furthermore, this adhesion layer has nothing to do with surface roughness due to the planarization process.

The adhesion layer, which the Examiner considers to be the thin film defined by Claim 4, is not formed of the same material as the electrode. Instead, in the Zurcher et al.

patent, the barrier layer 208 is TiN or TaN, the adhesion layer is Ti or Ta, and the electrode is described at column 7, lines 7-8, as being the same as electrode 70, which is described at column 3, lines 19-30, of the Zurcher et al. patent. The list of possible materials used for the electrode at this section of the Zurcher et al. patent does not appear to match the material described for either the barrier layer or the adhesion layer.

The Appellant maintains that the thin film in Claim 4 is between the lower electrode 26 and the dielectric or ferroelectric layer 28 and not under the lower electrode, and that the Zurcher et al. patent does not meet this limitation.

Claim 4 also includes structural features previously discussed with respect to Claim 1 that are not found in the disclosures of the Onishi patent, the Knight et al. patent, and the Zurcher et al. patent, taken alone or in combination. More specifically, Claim 4 calls for the concave portion or hollow 14 being formed at the top surface of insulation film 12 such that the lower electrode layer 16 is brought into contact with the bottom surface of the concave portion or hollow 14. As stated previously with respect to Claim 1, the contact hole or through-hole described in *Onishi* extends completely through the insulation films 2, 7. Therefore, *Onishi* does not describe "an insulation film having a concave portion at a top surface", but rather insulation films with contact holes, as described at column 8, lines 14-15, 24-26, and 30-32, which extend entirely through the insulation films 2, 7 down to the substrate 1. The Knight et al. patent shows no contact holes or hollows in the structure of the polymeric electrolyte, and does not even relate to art which would be considered analogous to that in which Appellant's claimed invention resides. The Zurcher et al. patent clearly shows openings 240 that extend all the way down to barrier layer 208 and contact plug 204, as shown in FIG. 11 and described at column 6, lines 8-43, of the Zurcher et al. patent.

Also, Claim 4 includes the limitation that a side of the thin film, a side of the ferroelectric layer, and a side of the upper electrode layer are flush with each other. As stated previously with respect to Claim 1, the Onishi patent does not disclose this structure. In *Onishi*, the sides of the upper electrode layer 10, as shown in Figure 7, are not

flush with sides of the ferroelectric layer 9, layer 8a, or layer 8b. The Knight et al. patent shows no comparable structure. The Zurcher et al. patent does not show a laminated body formed of layers each of which has a side which is flush with the sides of the other layers, as clearly shown in FIG. 11 of the Zurcher et al. patent

Consequently, for the foregoing reasons, neither the Onishi patent, nor the Knight et al. patent, nor the Zurcher et al. patent, taken alone or in combination, teach esor suggests the limitations of Claim 4. In that the Examiner has failed to establish that Claim 4 is unpatentable over the prior art, the rejection of Claim 4 under 35 U.S.C. 103(a) as being unpatentable over Onishi in view of Knight et al. and further in view of Zurcher et al. is improper, and should be withdrawn.

Claim 5

(D) Claim 5 is patentable under 35 U.S.C. §103(a) over Onishi modified by Knight et al., as applied to Claim 1, and further in view of Hanagasaki (US 5,767,541, issued June 16, 1998).

Claim 5 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over the Onishi patent modified by the Knight, et al. patent as applied to Claim 1, and further in view of U.S. Patent No. 5,767,541 (Hanagasaki). With respect to Claim 5, the Examiner acknowledges in the Final Office Action of December 3, 2003 that the Onishi patent does not disclose that the top surfaces of the lower electrode and the insulating film are planarized flush with each other. However, the Examiner contends that the Hanagasaki patent discloses a lower electrode which is planarized flush with the insulating film, and refers to Figure 1E of the Hanagasaki patent for showing this. The Examiner further contends that the Hanagasaki patent discloses that planarization could remove surface irregularities, and refers to Column 7, line 37 of the Hanagasaki patent for disclosing this. The Examiner concludes, therefore, that it would have been obvious for one with ordinary skill in the art to modify the Onishi structure with the teaching of the Hanagasaki patent to planarize the top surface of the lower electrode flush with the insulating film in order to remove the surface irregularities.

Figure 7 of the pending application discloses one of the features of the claim being that the top surface of the lower electrode 26 is planarized flush with the top surface of the insulating film 12, and, therefore, the lower electrode 26 is entirely buried in the hole 14. This shortens the etch time, because no portion of lower electrode 26 extends out of the hole and needs to be etched.

In the Final Office Action of December 9, 2003, the Examiner agreed that the Onishi patent does not show this feature, but he cited the Hanagasaki patent as disclosing the lower electrode as being planarized flush with the insulating film, and he refers to Figure 1E of the Hanagasaki patent for showing this feature.

The Appellant maintains that in the Hanagasaki patent, and in particular Figure 1E, the reference numeral 8 actually refers to the W plug (i.e., a tungsten plug), and Column 7, line 30 of the Hanagasaki patent describes this. The Appellant maintains that the electrode is actually reference numeral 9A and is shown in Figure 1G, and electrode 9A is actually on top of insulating film 7, and does not have a planarized top surface which is flush with the top surface of insulating film 7.

If the Examiner contends that the W plug is part of the electrode, this cannot be, as the W plug is separate from the electrode which is described in the Hanagasaki patent as being reference number 9A, and further that the top surface of the electrode is not planarized flush with the top surface of insulating film 7. The Knight et al. patent also does not disclose comparable structure, and was only cited by the Examiner for teaching a vacuum drying gel method.

Accordingly, it is respectfully urged that the particular structure set forth in Claim 5 is not taught or suggested by the Onishi patent, the Knight et al. patent and the Hanagasaki patent, alone or in combination, and is allowable.

Claim 5 also includes structural features previously discussed with respect to Claim 1 that are not found in the disclosures of the Onishi patent, the Knight et al. patent, and the Hanagasaki patent, taken alone or in combination. More specifically, Claim 4 calls for the

concave portion or hollow 14 being formed at the top surface of insulation film 12 such that the lower electrode layer 16 is brought into contact with the bottom surface of the concave portion or hollow 14. As stated previously with respect to Claim 1, the contact hole or through-hole described in *Onishi* extends completely through the insulation films 2, 7. Therefore, *Onishi* does not describe "an insulation film having a concave portion at a top surface", but rather insulation films with contact holes, as described at column 8, lines 14-15, 24-26, and 30-32, which extend entirely through the insulation films 2, 7 down to the substrate 1. The Knight et al. patent shows no contact holes or hollows in the structure of the polymeric electrolyte, and does not even relate to art which would be considered analogous to that in which Appellant's claimed invention resides. The Hanagasaki patent shows no comparable structure of a hollow or concave portion being formed in a top surface of an insulating film, as is clear from FIGS. 1E through 1G of the Hanagasaki patent.

Also, Claim 5 includes the limitation that a side of the ferroelectric layer, and a side of the upper electrode layer are flush with each other. As stated previously with respect to Claim 1, the Onishi patent does not disclose this structure. In *Onishi*, the sides of the upper electrode layer 10, as shown in Figure 7, are not flush with sides of the ferroelectric layer 9, layer 8a, or layer 8b. The Knight et al. patent shows no comparable structure. The Hanagasaki patent does not show a laminated body formed of layers each of which has a side which is flush with the sides of the other layers, as clearly shown in FIGS. 1A-1H, FIGS. 2, 3, 4A and 4B, and 5A and 5B of the Hanagasaki patent.

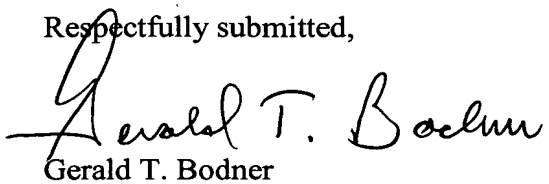
In that the Examiner has failed to establish that Claim 5 is unpatentable over the prior art, the rejection of Claim 5 under 35 U.S.C. 103(a) as being unpatentable over Onishi in view of Knight et al. and further in view of Hanagasaki is improper, and should be withdrawn.

CONCLUSION

In view of the arguments submitted hereinabove, the references applied against Claims 1 and 3-5 on appeal do not render those claims unpatentable under 35 U.S.C. §103.

Thus, Appellant respectfully submits that the rejections over the prior art are in error and must be reversed.

Respectfully submitted,



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APPENDIX

CLAIMS ON APPEAL: CLAIMS 1 AND 3-5

1. A ferroelectric memory, comprising:

an insulation film having a concave portion at a top surface; and

a laminated body obtained by laminating a plurality of layers on said top surface and etching a region of said plurality of layers corresponding to a region other than said concave portion, wherein

said laminated body includes a lower electrode layer which is made of a gel dry film and brought into contact with a bottom surface of said concave portion, a ferroelectric layer formed on said lower electrode layer and an upper electrode layer formed on said ferroelectric layer, wherein

a portion of said lower electrode layer is only embedded in said concave portion, and protrudes outward from an inner peripheral edge forming said concave portion, and a side of said portion of said lower electrode layer, a side of said ferroelectric layer and a side of said upper electrode layer are flush with each other.

2. (Cancelled)

3. A ferroelectric memory, comprising:

an insulation film having a hollow at a top surface; and

a laminated body obtained by laminating a plurality of layers on said top surface and etching a region of said plurality of layers corresponding to a region other than said hollow, wherein

said laminated body includes a lower electrode layer, a ferroelectric layer formed on said lower electrode layer and an upper electrode layer formed on said ferroelectric layer, and

said lower electrode layer includes a first electrode portion formed by a sol-gel technique only at a corner of said hollow and a second portion formed on said first electrode portion.

4. A ferroelectric memory, comprising:

an insulation film having a concave portion at a top surface; and

a laminated body obtained by laminating a plurality of layers on said top surface and etching a region of said plurality of layers corresponding to a region other than said concave portion, wherein

said laminated body includes a lower electrode layer which is brought into contact with a bottom surface of said concave portion, thin film of a same material as that of said lower electrode layer formed on a surface of said lower electrode layer, a ferroelectric layer formed on said thin film and an upper electrode layer formed on said ferroelectric layer, and a side of said thin film, a side of said ferroelectric layer and a side of said upper electrode layer are flush with each other.

5. A ferroelectric memory, comprising:

an insulation film having a concave portion at a top surface; and

a laminated body obtained by laminating a plurality of layers on said top surface and etching a region of said plurality of layers corresponding to a region other than said concave portion, wherein

said laminated body includes a lower electrode layer which is brought into contact with a bottom surface of said concave portion, a ferroelectric layer formed on said lower electrode layer and an upper electrode layer formed on said ferroelectric layer, wherein

said lower electrode layer and said insulation film at respective top surfaces are planarized flush with each other, and a side of said ferroelectric layer and a side of said upper electrode layer are flush with each other.